Octal 14-Bit, Parallel Input, Voltage-Output DAC

Prelim Technical Information

AD7841

FEATURES

Eight 14-Bit DACs in One Package
Voltage Outputs
Offset Adjust for Each DAC Pair
Reference Range of ±5 V
Maximum Output Voltage Range of ±10 V
Clear Function to User-Defined Voltage
44-Pin PQFP Package

APPLICATIONS

Process Control
Automatic Test Equipment
General Purpose Instrumentation

GENERAL DESCRIPTION

The AD7841 contains eight 14-bit DACs on one monolithic chip. It has output voltages with a full-scale range of ±10 V from reference voltages of ±5 V.

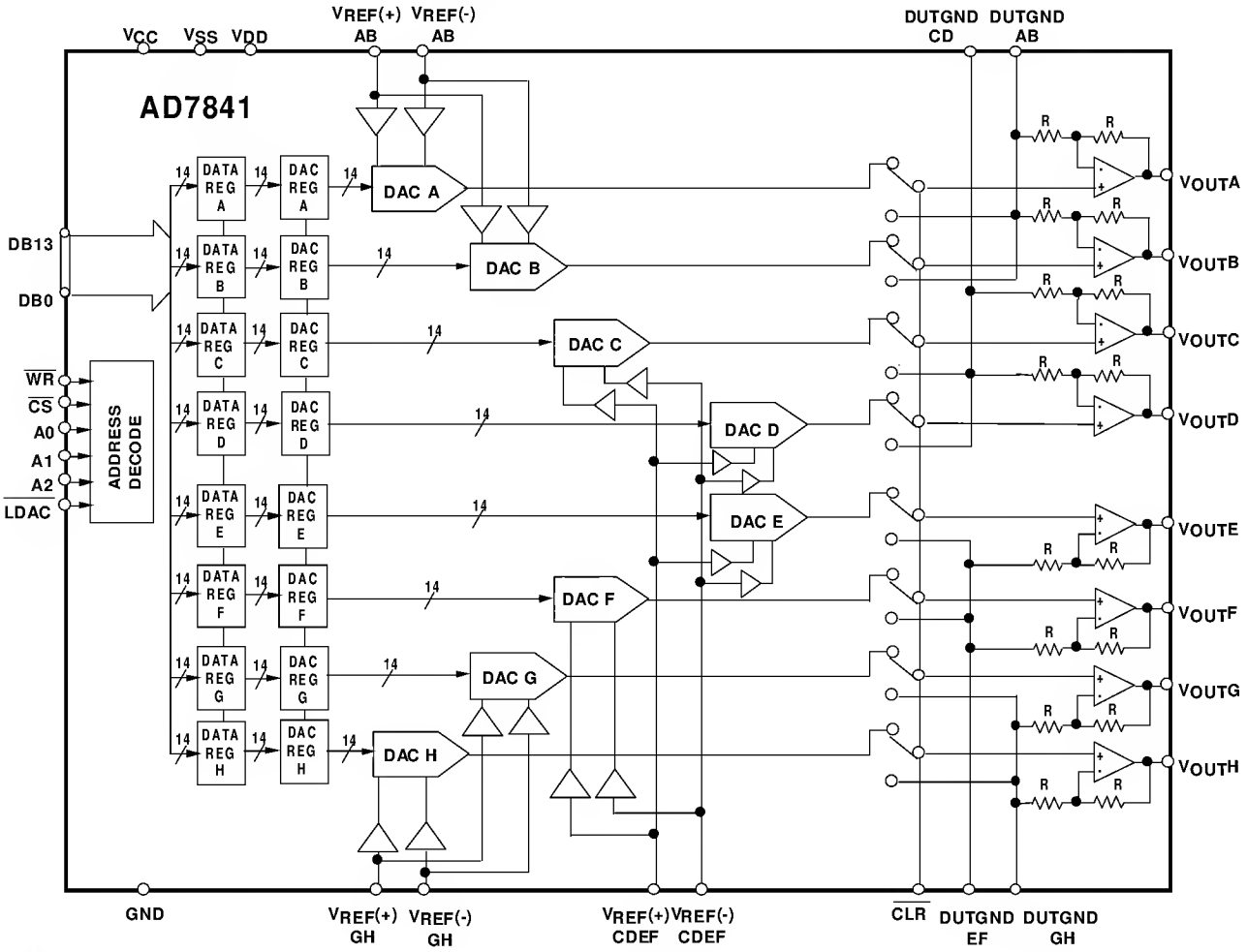
The AD7841 accepts 14-bit parallel loaded data from the external bus into one of the input latches under the control of the $\overline{WR}$, $\overline{CS}$ and DAC channel address pins, A0–A2.

The DAC outputs are updated on reception of new data into the DAC registers. All the outputs may be updated simultaneously by taking the $\overline{LDAC}$ input low.

Each DAC output is buffered with a gain-of-two amplifier into which an external DAC offset voltage can be inserted via the DUTGNDx pins.

The AD7841 is available in a 44-pin PQFP package.

FUNCTIONAL BLOCK DIAGRAM



PRELIM A 9/97

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD7841–SPECIFICATIONS

(V_{CC} = +5 V ±5%; V_{DD} = +15 V ± 5%; V_{SS} = -15 V ± 5%; GND = DUTGND = 0 V; R_L = 5 kΩ and C_L = 50 pF to GND, T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A	Units	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy	±4	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic Over Temperature
Zero-Scale Error	±8	LSB max	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V. Typically within ±2 LSB
Full-Scale Error	±8	LSB max	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V. Typically within ±2 LSB
Gain Error	±4	LSB typ	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V
Gain Temperature Coefficient[2]	20	ppm FSR/°C typ	
	40	ppm FSR/°C max	
DC Crosstalk[2]	50	µV max	See Terminology.
REFERENCE INPUTS[2]			
DC Input Resistance	100	MΩ typ	
Input Current	±1	µA max	Per Input. Typically ±20 nA
$V_{REF}(+)$ Range	0/+5	V min/max	
$V_{REF}(-)$ Range	–5/0	V min/max	
$[V_{REF}(+) - V_{REF}(-)]$	+2/+10	V min/max	For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed
DUTGND INPUTS[2]			
DC Input Impedance	60	kΩ typ	
Input Current	±0.3	mA max	Per Input. Typically
Input Range	-2/+2	V min/max	
OUTPUT CHARACTERISTICS			
Output Voltage Swing	±10	V min	$2 \times (V_{REF}(-) + [V_{REF}(+) - V_{REF}(-)] \cdot D) - V_{DUTGND}$
Short Circuit Current[2]	15	mA max	
Resistive Load	5	kΩ min	To 0 V
Capacitive Load	50	pF max	To 0 V
DC Output Impedance[2]	0.5	Ω max	
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±10	µA max	Total for All Pins
C_{IN}, Input Capacitance[2]	10	pF max	
POWER REQUIREMENTS			
V_{CC}	5.0	V nom	±5% for Specified Performance
V_{DD}	15.0	V nom	±5% for Specified Performance
V_{SS}	–15.0	V nom	±5% for Specified Performance
Power Supply Sensitivity			
ΔFull Scale/ΔV_{DD}	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	dB typ	
I_{CC}	0.5	mA max	$V_{INH} = V_{CC}$, V_{INL} = GND. Dynamic Current
	8	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max
I_{DD}	14	mA max	Outputs Unloaded. Typically 7 mA
I_{SS}	14	mA max	Outputs Unloaded. Typically 7 mA

NOTES
[1]Temperature range for A Version: –40°C to +85°C
[2]Guaranteed by characterization. Not production tested.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to production testing.)

Parameter	A	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	20	µs typ	Full-Scale Change to ±1/2 LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Slew Rate	1.5	V/µs typ	
Digital-to-Analog Glitch Impulse	120	nV-s typ	Measured with $V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V. DAC Latch Alternately Loaded with 0FFF Hex and 1000 Hex. Not Dependent on Load Conditions
Channel-to-Channel Isolation	100	dB typ	See Terminology
DAC-to-DAC Crosstalk	3	nV-s typ	See Terminology
Digital Crosstalk	3	nV-s typ	Feedthrough to DAC Output Under Test Due to Change in Digital Input Code to Another Converter
Digital Feedthrough	3	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density @ 1 kHz	65	nV/(Hz)$^{1/2}$ typ	All 1s Loaded to DAC. $V_{REF}(+) = V_{REF}(-)$ = 0 V

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{CC} = +5 V ± 5%; V_{DD} = +15 V ± 5%; V_{SS} = -15 V ± 5 %; GND = DUTGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
t_1	15	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	50	ns min	$\overline{CS}$ Pulse Width Low
t_4	50	ns min	$\overline{WR}$ Pulse Width Low
t_5	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_6	0	ns min	$\overline{WR}$ to $\overline{CS}$ Hold Time
t_7	15	ns min	Data Setup Time
t_8	0	ns min	Data Hold Time
t_9	20	µs typ	Settling Time
t_{10}	300	ns max	$\overline{CLR}$ Pulse Activation Time
t_{11}	50	ns min	$\overline{LDAC}$ Pulse Width Low

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Rise and fall times should be no longer than 50 ns.
Specifications subject to change without notice.

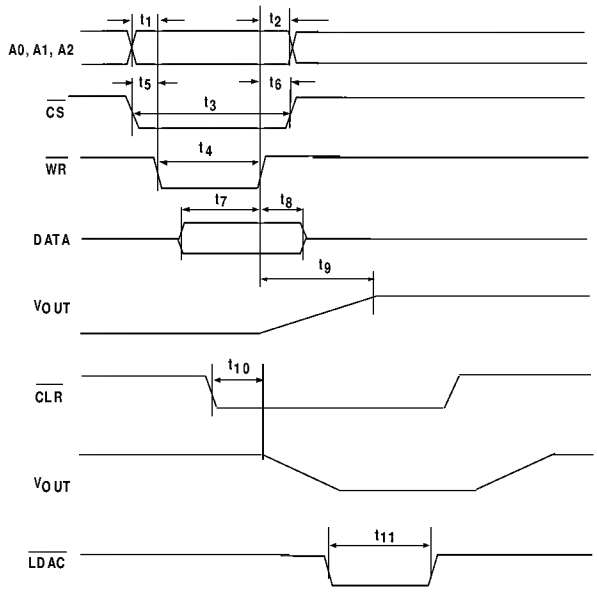


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{CC} to GND ..... –0.3 V, +7 V or V_{DD} + 0.3 V (Whichever Is Lower)
V_{DD} to GND ..... –0.3 V, +17 V
V_{SS} to GND ..... +0.3 V, –17 V
Digital Inputs to GND ..... –0.3 V, V_{CC} + 0.3 V
V_{REF}(+) to V_{REF}(-) ..... –0.3 V, +18 V
V_{REF}(+) to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{REF}(-) to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
DUTGND to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{OUT}(A–H) to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
PQFP Package, Power Dissipation ..... 480 mW
θ_{JA} Thermal Impedance ..... 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

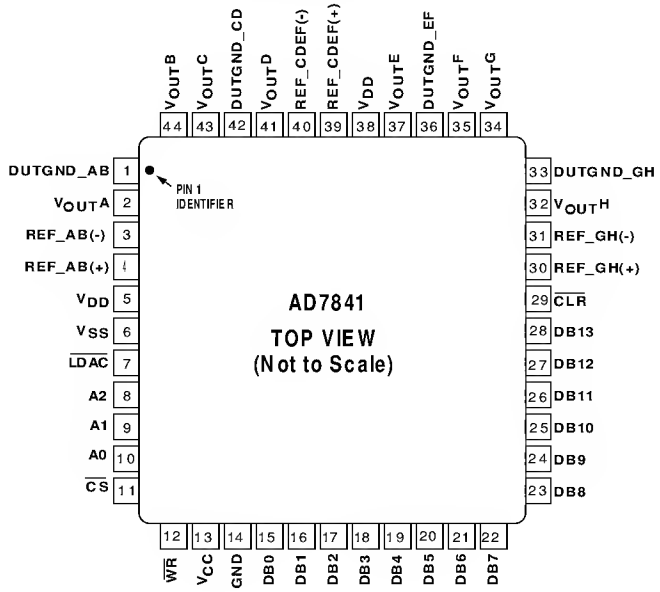
Model	Temperature Range	Linearity Error (LSBs)	DNL (LSBs)	Package Option*
AD7841AS	–40°C to +85°C	±4	±1	S-44

*S = Plastic Quad Flatpack (PQFP).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7841 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN DESCRIPTION

Pin Mnemonic	Description
V_{CC}	Logic Power Supply; +5 V ± 5%.
V_{SS}	Negative Analog Power Supply; -15 V ± 5%.
V_{DD}	Positive Analog Power Supply; +15 V ± 5%.
GND	Ground.
$V_{REF}(+)AB$, $V_{REF}(-)AB$	Reference Inputs for DACs A and B. These reference voltages are referred to GND.
$V_{REF}(+)CDEF$, $V_{REF}(-)CDEF$	Reference Inputs for DACs C, D, E and F. These reference voltages are referred to GND.
$V_{REF}(+)GH$, $V_{REF}(-)GH$	Reference Inputs for DACs G and H. These reference voltages are referred to GND.
$V_{OUT}A$ . . $V_{OUT}H$	DAC Outputs.
$\overline{CS}$	Level-Triggered Chip Select Input (active low). The device is selected when this input is low.
DB0 . . DB13	Parallel Data Inputs. The AD7841 can accept a straight 14-bit parallel word on DB0 to DB13 where DB13 is the MSB and DB0 is the LSB.
A0, A1, A2	Address inputs. A0, A1 and A2 are decoded to select one of the eight input data registers for a data transfer.
$\overline{LDAC}$	Load DAC Logic Input (active low). When this logic input is taken low the contents of the input latches are transferred to their respective DAC latches.
$\overline{CLR}$	Asynchronous Clear Input (level sensitive, active low). When this input is low, all analog outputs are switched to the externally set potential on the relevant DUTGND pin. The contents of data registers and DAC registers A to H are not affected when the $\overline{CLR}$ pin is taken low. When $\overline{CLR}$ is brought back high, the DAC outputs revert back to their original outputs as determined by the data in their DAC registers.
$\overline{WR}$	Level-Triggered Write Input (active low), used in conjunction with $\overline{CS}$ to write data to the AD7841 input data registers. Data is latched into the selected data register on the rising edge of $\overline{WR}$.
DUTGND AB	Device Sense Ground for DACs A and B. Vout A and Vout B are referenced to the voltage applied to this pin.
DUTGND CD	Device Sense Ground for DACs C and D. Vout C and Vout D are referenced to the voltage applied to this pin.
DUTGND EF	Device Sense Ground for DACs E and F. Vout E and Vout F are referenced to the voltage applied to this pin.
DUTGND GH	Device Sense Ground for DACs G and H. Vout G and Vout H are referenced to the voltage applied to this pin.